Rapid Prototyping of Application-Specific Signal Processors

Alta Group of Cadence Design Systems

The Alta Group will integrate the Signal Processing WorkSystem (SPW) and the Block Oriented Network Simulator (BONeS) into the RASSP design environment. The functionality of SPW will then be extended by creating interfaces to other tools.

Focus on RASSP

Alta Group will incorporate the full functionality of SPW into the RASSP design environment. SPW is a powerful software package for interactive design, simulation, and implementation of digital signal processing (DSP) and communications systems. As part of its tightly integrated core system, SPW offers a range of features and capabilities that greatly speed pivotal parts of the design process:

- An intuitive user interface
- Ability to capture and effortlessly implement system-level block diagrams
- Digital filter design
- Powerful waveform capture, generation, editing, transformation, and analysis

- Hardware and software prototyping
- Design reusability
- Open design database.

In SPW, users graphically specify a DSP algorithm by the placement and interconnection of adders, multipliers, FFTs, delays, quantizers, etc. from more than 600 signal processing blocks.

Once the design is captured, a built-in simulator exercises the design, causing it to perform the way an actual DSP system would. Simulation results quickly reveal any difficulties in the design, and help users make the necessary revisions or adjustments.
Co-simulation: SPW block diagram with embedded MATLAB FM modulator function.

SPW’s application-oriented libraries offer focused, market-specific expertise across these DSP and communications applications: wireless and satellite communications, modems, mobile radios, cellular phones, radar, sonar, speech encoding, image processing, digital audio, multimedia, automotive electronics, robotics, neural nets, HDTV, biomedical systems, countermeasures, and test and measurement.

Alta Group will integrate SPW with JRS’ Network Synthesis System (NetSyn) to enable the transfer of SPW designs into NetSyn, and then reduce those designs into multiprocessor hardware implementations. Alta Group will develop an SPW/MATLAB interface that will allow MATLAB ‘.m’ files to be included in an SPW block-diagram, where they will be treated similarly to a native SPW library block.

The Block Oriented Network Simulator (BONEs) DESIGNER is a graphical framework for transaction-based modeling of communication networks, distributed computer systems, and computer architectures. Alta Group will integrate DESIGNER into the RASSP design environment to enable users to simulate and verify the performance of the proposed system.

DESIGNER consists of several tightly integrated tools operating in a common environment. The tools allow graphical definition of data structures and models, specification of simulation parameters and performance metrics, and the post-simulation analysis and display of results. The interactive simulation tool allows visualization and modification of a simulation as it executes.

In a DESIGNER model, Data Structures represent packets, messages, or transactions that flow through a system of shared resources, protocols, and algorithms. DESIGNER’s core libraries allow modeling of shared resources, such as processors, memories, buses, and communication channels. Users can extend the core libraries by creating new modules graphically using existing modules, or with the C programming language.

For More Information
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